Notice of References Cited	Application/Control No. 10/708,268	Applicant(s)/Patent Under Reexamination SAMUDRALA ET AL.	
	Examiner Daniel D. Chang	Art Unit 2819	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Carmichael et al., "SEU Mitigation Techniques for Virtex FPGAs in Space Applications", 1999 MAPLD Conference, pp. 1-21
	V	Brindley et al. "SEU Mitigation Design Techniques for the XQR4000XL", Xilinx, XAPP181 (v1.0) March 15, 2000
	W	Carmichael, "Triple Module Redundancy Design Techniques for Virtex FPGAs", Xilinx, XAPP197 (v1.0) November 1, 2001
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.